WHAT IS CLAIMED IS:

1. A semiconductor device, comprising:

a substrate;

transistors formed on the substrate, each of the transistors including a channel formation region to form a channel between a source region and a drain region; and

a gate electrode facing the channel formation region with a gate insulating film interposed therebetween,

at least a part of the gate insulating film overlapping with a boundary region of the channel formation region adjacent to the drain region, being thicker than a part of the gate insulating film overlapping with a center part of the channel formation region, relative to a longitudinal direction of the channel.

2. The semiconductor device according to Claim 1, a part of the gate insulating film overlapping with a boundary region of the channel formation region adjacent to the source region, being thicker than the part of the gate insulating film overlapping with the center part of the channel formation region, relative to the longitudinal direction of the channel.

3. The semiconductor device according to Claim 1, each of the source region and the drain region having a lightly doped region or an offset region facing the gate electrode with the gate insulating film interposed therebetween; and

at least a part of the gate insulating film overlapping with a boundary region of the channel formation region adjacent to the lightly doped region or the offset region of the drain region, being thicker than the part of the gate insulating film overlapping with the center part of the channel formation region, relative to the longitudinal direction of the channel.

4. The semiconductor device according to Claim 3, a part of the gate insulating film overlapping with a boundary region of the channel formation region adjacent to the lightly doped region or the offset region of the source region, being thicker than the part of the gate insulating film overlapping with the center part of the channel formation region, relative to the longitudinal direction of the channel.

5. The semiconductor device according to Claim 1, the channel formation region, the source region, and the drain region being formed on a semiconductor film formed on a surface of the substrate.

6. The semiconductor device according to Claim 1, the substrate being a semiconductor substrate, and the channel formation region, the source region, and the drain region being formed on the semiconductor substrate.

7. An electro-optical device including the semiconductor device, according to Claim 1 as a substrate for an electro-optical device holding an electro-optical material,

pixels, each including a pixel switching transistor and a pixel electrode, being formed on the substrate for the electro-optical device in a matrix.

8. The electro-optical device according to Claim 7, the electro-optical material being liquid crystal held between the substrate for the electro-optical device and a counter substrate.

9. The electro-optical device according to Claim 7, the electro-optical material being an organic electroluminescent material constituting a light-emitting device on the substrate for the electro-optical device.

10. An electronic apparatus using the electro-optical device according to Claim 7.

11. A method for manufacturing a semiconductor device in which transistors are formed on a substrate, each of the transistors including a channel formation region to form a channel between a source region and a drain region, and a gate electrode facing the channel formation region with a gate insulating film interposed therebetween, the method including a step of forming the gate insulating film,

the step of forming the gate insulating film, comprises:

forming a lower-layer gate insulating film,

forming a resist layer on at least a part of the surface of the lower-layer gate insulating film overlapping with a center part of the channel formation region relative to the longitudinal direction of the channel, and not forming the resist layer on at least a part of the surface of the lower-layer gate insulating film overlapping with a boundary region of the channel formation region adjacent to the drain region,

forming an upper-layer gate insulating film on surfaces of the lower-layer gate insulating film and the resist layer, and

removing the resist layer together with the upper-layer gate insulating film formed thereon.

12. The method according to Claim 11, the resist layer not being formed on a part of the surface of the lower-layer gate insulating film overlapping with a boundary region of the channel formation region adjacent to the source region.

13. A method for manufacturing a semiconductor device in which transistors are formed on a substrate, each of the transistors including a channel formation region to form a channel between a source region and a drain region, and a gate electrode facing the channel

formation region with a gate insulating film interposed therebetween, the method including forming the gate insulating film,

the step of forming the gate insulating film, comprising:

forming a resist layer on at least a part overlapping with a center part of the channel formation region relative to the longitudinal direction of the channel, and not forming the resist layer on at least a part overlapping with a boundary region of the channel formation region adjacent to the drain region,

forming a lower-layer gate insulating film on the surface side of the resist layer,

removing the resist layer together with the lower-layer gate insulating film formed thereon, and

forming an upper-layer gate insulating film on a surface of the lower-layer gate insulating film.

14. The method according to Claim 13, the resist layer not being formed on a part overlapping with a boundary region of the channel formation region adjacent to the source region.

15. A method for manufacturing a semiconductor device in which transistors are formed on a substrate, each of the transistors including a channel formation region to form a channel between a source region and a drain region, and a gate electrode facing the channel formation region with a gate insulating film interposed therebetween, the source region and the drain region each having a lightly doped region or an offset region facing the gate electrode with the insulating film interposed therebetween, the method including forming the gate insulating film,

forming the gate insulating film, comprising:

forming a lower-layer gate insulating film,

forming a resist layer on at least a part of the surface of the lower-layer gate insulating film overlapping with a center part of the channel formation region relative to the longitudinal direction of the channel, and not forming the resist layer on at least a part of the surface of the lower-layer gate insulating film overlapping with a boundary region of the channel formation region adjacent to the lightly doped region or the offset region of the drain region,

forming an upper-layer gate insulating film on surfaces of the lower-layer gate insulating film and the resist layer, and

removing the resist layer together with the upper-layer gate insulating film formed thereon.

16. The method according to Claim 15, the resist layer not being formed on a part overlapping with a boundary region of the channel formation region adjacent to the lightly doped region or the offset region of the source region.

17. A method for manufacturing a semiconductor device in which transistors are formed on a substrate, each of the transistors including a channel formation region to form a channel between a source region and a drain region, and a gate electrode facing the channel formation region with a gate insulating film interposed therebetween, the source region and the drain region each having a lightly doped region or an offset region facing the gate electrode with the insulating film interposed therebetween, the method including forming the gate insulating film,

forming the gate insulating film, comprising:

forming a resist layer on at least a part overlapping with a center part of the channel formation region relative to the longitudinal direction of the channel, and not forming the resist layer on at least a part overlapping with a boundary region of the channel formation region adjacent to the lightly doped region or the offset region of the drain region,

forming a lower-layer gate insulating film on the surface side of the resist layer,

removing the resist layer together with the lower-layer gate insulating film formed thereon, and

forming an upper-layer gate insulating film on a surface of the lower-layer gate insulating film.

18. The method according to Claim 17, the resist layer not being formed on a part overlapping with a boundary region of the channel formation region adjacent to the lightly doped region or the offset region of the source region.